AMENDMENTS TO THE CLAIMS

A detailed listing of all claims that are, or were, in the present application, irrespective of whether the claim(s) remains under examination in the application are presented below. The claims are presented in ascending order and each includes one status identifier. Those claims not cancelled or withdrawn but amended by the current amendment utilize the following notations for amendment: 1. deleted matter is shown by strikethrough for six or more characters and double brackets for five or less characters; and 2. added matter is shown by underlining.

1. (Currently Amended) A method of calculating a [[the]] fast Fourier transform or an [[the]] inverse fast Fourier transform of a digital signal defined by a series of N real starting samples x(n), with N a power of two and n ∈ [0..N-1], the method comprising the steps of: ~~successive transformation steps (2) for~~

transforming input samples into output samples in a first transformation step;[[,]]

transforming input samples into output samples in at least one successive transformation step to the first transformation step; and

storing the input samples and output samples of each transformation step in a storage memory;

wherein each of [[all]] the transformation steps is [[being]] performed by means of a single set of butterfly circuits ~~butterflies~~ with several inputs and several outputs, the operating mode of the set of butterfly circuits ~~which is~~ modified selectively in each transformation step, ~~the input and output samples of each transformation step being stored in a storage memory,~~ a series of N output samples y(n) representative of the fast Fourier transform or the inverse fast Fourier transform of the output samples x(n) being provided in a [[the]] last transformation step;[[,]]

wherein ~~characterized in that~~ output samples y(n) are real;[[,]]

[[and]] wherein [[that]] output samples of a butterfly circuit replace the corresponding input samples of the same rank in the storage memory, so that, if the starting samples ~~examples~~ x(n) processed in the first transformation step are classified in bit-reversed order of their index n, output samples y(n) are provided in the last transformation step in ascending order of index n and are~~, these output samples being~~ defined by the following relations:

y (0) = Re [X (0)],

y (n) = Re [X ((n+1) /2] for n being odd and different from N-1,

y (n) = Im[X (n/2)] for n being even and different from 0, and

y (N-1) = Re [X (N/2)]; and

wherein samples X (n), with n ∈ [0..N-1], designate [[the]] complex samples of the series corresponding to the fast or inverse fast Fourier transform of the starting samples series x(n).

2. (Currently Amended) A method of calculating a [[the]] fast Fourier transform or an [[the]] inverse fast Fourier transform of a digital signal defined by a series of N complex samples X(n) conjugated by pairs, characterized in that the calculation is done on a series of N real starting samples y(n) representative of the series of complex samples X(n), with N power of two and n c [0..N-1], the starting samples y(n) being defined as follows:

y(0) = Re[X(0)],

y(n) = Re[X((n+l)/2)] for n being odd and different from N-1,

y(n) = Im[X(n/2)] for n being even and different from 0, and

y(N-1) = Re[X(N/2)];

~~in that this~~ the method comprising the steps of: ~~comprises successive~~

~~transformation steps for~~

transforming input samples into output samples in a first transformation step;[[,]]

transforming input samples into output samples in at least one successive transformation step; and

storing the input samples and output samples of each transformation step in a storage memory;

wherein a series of N real output samples x(n) representative of the [[this]] fast or inverse fast Fourier transform is [[being]] provided in [[the]] a last transformation step, all of the transformation steps being performed by means of a single set of butterfly circuits ~~butterflies~~ with several inputs and several outputs, the operating mode of the set of butterfly circuits ~~which is~~ modified selectively in each successive transformation step;~~, the input and output samples of each transformation step being stored in a storage memory,~~

and wherein [[that]] the output samples of a butterfly circuit replace the corresponding input samples of the same rank in the storage memory, so that, if the starting samples y(n) processed in the first transformation step are classified in ascending order of index n, the output samples x(n) are provided in the last transformation step in bit-reversed order of index n.

3. (Currently Amended) The calculation method according to claim 1, wherein ~~characterized in that~~, in each transformation step, each butterfly circuit transforms input sample pairs, the ranks of the input samples of the same pair within the series of input samples of said transformation step being symmetrical with respect to a center between the end rank values of

the input samples transformed by said butterfly circuit.

4. (Currently Amended) The calculation method according to claim 3, further comprising the step of:

transforming input samples into output samples in ~~characterized in that it comprises~~ μ-1 transformation steps E_P, wherein [[with]] $\mu = \log_2 (N)$ and $p \in [\,0\,..\,\mu\,-2]$.

5. (Currently Amended) The calculation method according to claim 4, ~~characterized in~~ further comprising:

a preliminary step of modifying the sequence of the starting samples x(n) ranked in ascending order of index n and showing the starting samples [[them]] in bit-reversed order of index n in the first transformation step, and

a final step of processing the series of output samples y(n) and providing a series of N complex conjugated samples X(n) corresponding to the fast or the inverse fast Fourier transform of the series of starting samples x(n).

6. (Currently Amended) The calculation method of claim 4, wherein ~~characterized in that~~, in each transformation step E_P, butterfly circuits ~~butterflies~~ are distributed among $N/2^{P+2}$ calculation blocks,

wherein [[that]] each calculation block has a peripheral butterfly circuit and/or 2^P-1 internal butterfly circuits ~~butterflies~~,

wherein [[that]] the peripheral butterfly circuit of a [[the]] rank α calculation block in transformation step $E\beta$ transforms the input samples of rank $2^{\beta+2}\alpha$, $2^{\beta+2}\alpha+2^{\beta+1}$-

1, $2^{\beta+2}\alpha+2^{\beta+1}$, $2^{\beta+2}\alpha+2^{\beta+2}$-1 into output samples of the same rank,

and wherein [[that]] an [[the]] internal rank τ butterfly circuit of the rank α calculation block in transformation step Eβ transforms the input samples of rank $2^{\beta+2}\alpha+2\tau+1$, $2^{\beta+2}\alpha+2\tau+2$, $2^{\beta+2}\alpha+2^{\beta+2}-2\tau-3$, $2^{\beta+2}\alpha+2^{\beta+2}-2\tau-2$ into output samples of the same rank, with $\beta\geq 1$.

7. (Currently Amended) The calculation method according to claim 6, wherein ~~characterized in that~~ each butterfly circuit is assigned a coefficient W^S, whereon the calculation inside the butterfly circuit is based, wherein said coefficient is [[being]] equal to $e^{-j(2\pi s/N)}$ with s $\in$ [0..N/4-1] for a fast Fourier transform, and wherein said coefficient is equal to $e^{j(2\pi s/N)}$ with s $\in$ [0..N/4-1] for an inverse fast Fourier transform.

8. (Currently Amended) The calculation ~~Calculation~~ method according to claim 7, wherein ~~characterized in that~~ the internal rank τ butterfly circuit of the rank α calculation block in transformation step Eβ is assigned coefficient W^{δ} with $\delta=(\tau+1)\,.\,(N/2^{\beta+2})$.

9. (Currently Amended) The calculation method according to claim 8, wherein ~~characterized in that~~ the butterfly circuits ~~butterflies~~ for implementing the transformation steps are all of the same type and [[have]] comprise:

four inputs for receiving input samples and four outputs for providing output samples, and

four additional inputs, respectively primary mode, secondary mode, permutation,

and coefficient inputs,

~~in order~~ to selectively apply different transformation operations to the input samples, each operation being determined by the values assigned to the primary mode, secondary mode, permutation signals, and a coefficient admitted on said corresponding additional inputs.

10. (Currently Amended) The calculation method according to claim 9, wherein ~~characterized in that~~, for each butterfly circuit, the primary mode signal is 0 for a peripheral butterfly circuit and 1 for an internal butterfly circuit, and

wherein [[that]] the permutation signal is 0 for the even rank calculation blocks, including rank 0, and 1 for the other calculation blocks [[ones]].

11. (Currently Amended) The calculation method according to claim 10, wherein ~~characterized in that~~, in transformation step Ep, each calculation block comprises one peripheral butterfly circuit and 2^P-1 internal butterfly circuits ~~butterflies~~.

12. (Currently Amended) The calculation method according to claim 11, wherein ~~characterized in that~~ the secondary mode signal is 1 if the peripheral butterfly circuit is used for the last transformation step, and otherwise 0.

13. (Currently Amended) The calculation method according to claim 12, wherein ~~characterized in that~~, for four input samples el, e2, e3, and e4, and for a complex coefficient

W^S=A+j.B, the butterfly circuit delivers the following output samples s1, s2, s3, and s4:

1) if the primary mode and secondary mode signals are 0:

   s1 = e1+ e2,

   s2 = e1- e2,

   s3 = e4 - e3, and

   s4 = e3 + e4;

2) if the primary mode signal is 0 and the secondary mode signal is 1:

   s1 = e1 + e2 + e3 + e4,

   s2 = e1 - e2,

   s3 = e4 - e3, and

   s4 = (e1 + e2) - (e3 + e4);

3) if the primary mode signal is 1 and the permutation signal is 0:

   s1 = e1 + A.e3 - B.e4,

   s2 = e2 + B.e3 + A.e4,

   s3 = e1 - A.e3 + B.e4, and

   s4 = -e2 + B.e3 + A.e4; and

4) if the primary mode signal is 1 and the permutation signal is 1:

   s1 = e1 - A.e3 + B.e4,

   s2 = -e2 + B.e3 + A.e4,

   s3 = e1 - A.e3 - B.e4, and

   s4 = e2 + B.e3 + A.e4.

14. (Currently Amended) The calculation method according to claim 10, wherein ~~characterized in that~~, in transformation step E_P, each calculation block comprises:

2^P-1 internal butterfly circuits ~~butterflies~~ and a peripheral butterfly circuit for the even values of index p as well as for the last transformation step if μ is even, and

2^P-1 internal butterfly circuits ~~butterflies~~, otherwise.

15. (Currently Amended) The calculation method according to claim 13, wherein ~~characterized in that~~ the secondary mode signal is 1 if the peripheral butterfly circuit is used for the last transformation step with μ being odd, and otherwise 0.

16. (Currently Amended) The calculation method according to claim 15, wherein ~~characterized in that~~, for four input samples e1, e2, e3, and e4, and for a complex coefficient W^S=A+j.B, the butterfly circuit delivers the following output samples s1, s2, s3, and s4:

1) if primary mode, secondary mode and permutation signals are 0:

s1 = e1 + e2 + e3 + e4,

s2 = e1 - e2,

s3 = e4 - e3, and

s4 = (e1 + e2) - (e3 + e4);

2) if the primary mode signal is 0 and the secondary mode signal is 1:

s1 = e1 + e4,

s2 = e2,

s3 = e3, and

s4 = e1 - e4;

3) if the primary mode signal is 0 and the permutation signal is 1:

s1 = (e3 + e4) - (e1 + e2),

s2 = e1 - e2,

s3 = e4 - e3, and

s4 = e1 + e2 + e3 + e4;

4) if the primary mode signal is 1 and the permutation signal is 0:

s1 = e1 + A.e3 - B.e4,

s2 = e2 + B.e3 + A.e4,

s3 = e1 - A.e3 + B.e4, and

s4 = -e2 + B.e3 + A.e4; and

5) if the primary mode signal is 1 and the permutation signal is 1:

s1 = e1 - A.e3 + B.e4,

s2 = -e2 + B.e3 + A.e4,

s3 = e1 + A.e3 - B.e4, and

s4 = e2 + B.e3 + A.e4.

17. (Currently Amended) The calculation method according to claim 10, wherein ~~characterized in that~~, in transformation step E_P, each calculation block comprises:

2^P-1 internal butterfly circuits ~~butterflies~~ and a peripheral butterfly circuit for the even values of index p, and

2^P-1 internal butterfly circuits ~~butterflies~~, otherwise.

18. (Currently Amended) The calculation method according to claim 17, wherein ~~characterized in that~~ the secondary mode signal is 1 if the peripheral butterfly circuit is used for the first transformation step with μ being even, and otherwise 0.

19. (Currently Amended) The calculation method according to claim 18, wherein ~~characterized in that~~, for four input samples e1, e2, e3, and e4, and for a complex coefficient W^S=A+j.B, the butterfly circuit delivers the following output samples s1, s2, s3, and s4:

1) if the primary mode signal is 0 and the secondary mode signal is 1:

s1 = e1 + e2,

s2 = e1 - e2,

3 = 34 – e3, and

4 = e3 + e4;

2) if primary mode, secondary mode and permutation signals are 0:

s1 = e1 + e2 + e3 + e4,

s2 = e1 - e2,

s3 = e4 - e3, and

s4 = (e1 + e2) - (e3 + e4);

3) the primary mode and secondary mode signals the permutation signal is 1:

s1 = (e3 + e4) - (e1 + e2),

s2 = e1 - e2,

s3 = e4 - e3, and

s4 = e1 + e2 + e3 + e4;

4) if the primary mode permutation signal is 1 and the permutation signal is 0:

$s1 = e1 + A.e3 - B.e4$,

$s2 = e2 + B.e3 + A.e4$,

$s3 = e1 - A.e3 + B.e4$, and

$s4 = -e2 + B.e3 + A.e4$;

5) if the primary mode signal is 1 and the permutation signal is 1:

$s1 = e1 - A.e3 + B.e4$,

$s2 = -e2 + B.e3 + A.e4$,

$s3 = e1 + A.e3 - B.e4$, and

$s4 = e2 + B.e3 + A.e4$.

20. (Currently Amended) The calculation method according to claim 8, wherein ~~characterized in that~~ the butterfly circuits ~~butterflies~~ for implementing the transformation steps are all of the same type and [[have]] comprise:

[[-]]four inputs for receiving input samples and four outputs for providing output samples, and

[[-]]four additional inputs, respectively primary mode, secondary mode, permutation, and coefficient inputs,

~~in order~~ to selectively apply different transformation operations to the input samples, each operation being determined by the values assigned to the primary mode, secondary mode, permutation signals, and a coefficient admitted on said corresponding additional inputs,

and wherein [[that]] the final step furthermore performs an addition and subtraction between the first and the last output sample provided in the last transformation step.

21. (Currently Amended) The calculation method according to claim 20, wherein ~~characterized in that~~, in transformation step E_P, each calculation block comprises one peripheral butterfly circuit and 2^P-1 internal butterfly circuits ~~butterflies~~.

22. (Currently Amended) The calculation method according to claim 21, wherein ~~characterized in that~~, for four input samples e1, e2, e3, and e4, and for a complex coefficient W^S=A+j.B, the butterfly circuit delivers the following output samples s1, s2, s3, and s4:

1) if the primary mode signal is 0:

   s1 = e1 + e2,

   s2 = e1 - e2,

   s3 = e4 - e3, and

   s4 = e3 + e4;

2) if the primary mode signal is 1 and the permutation signal is 0:

   s1 = e1 + A.e3 - B.e4,

   s2 = e2 + B.e3 + A.e4,

   s3 = e1 - A.e3 + B.e4, and

   s4 = -e2 + B.e3 + A.e4;

3) if the primary signal is 1 and the permutation signal is 1:

s1 = e1 - A.e3 + B.e4,

s2 = -e2 + B. e3 + A. e4,

s3 = e1 + A.e3 -B.e4, and

s4 = e2 + B.e3 + A.e4.

23. (Currently Amended) The calculation method according to claim 9, wherein ~~characterized in that~~ the first and second binary addresses of μ bits are generated for each butterfly circuit, each binary address corresponding to the rank of an input sample of said butterfly circuit and the second binary address being greater than the first binary address.

24. (Currently Amended) The calculation method according to claim 23, wherein ~~characterized in that~~ said first and second binary addresses are consecutive and an internal butterfly circuit is involved.

25. (Currently Amended) The calculation method according to claim 23, wherein ~~characterized in that~~, if a peripheral butterfly circuit is involved, the p+2 low-order bits of the first address are equal to 0, and the p+2 low-order bits of the second address form a number equal to 2^{p+1}-1.

26. (Currently Amended) The calculation method according to claim 24, wherein ~~characterized in that~~ the addresses of [[the]] two other samples to be applied to the inputs of the

butterfly circuit, ~~be they~~ whether peripheral or internal, are obtained by inverting the (p+2) low-order bits of said first and second produced addresses.

27. (Currently Amended) The calculation method according to claim 26, wherein ~~characterized in that~~ even-numbered address samples and odd-numbered address samples are stored in two separate memories.

28. (Currently Amended) The calculation method according to claim 25, wherein ~~characterized in that~~ the value of the parameter s of the coefficient W^S assigned to an internal butterfly circuit in transformation step E_P is coded by μ-2 bits, and is:

[[-]]if p+1=μ-2, the number formed by the p+1 low-order bits of the second binary address produced for said internal butterfly circuit;[[,]]

[[-]]if p+1<μ-2, the number formed by the p+1 low-order bits of the second binary address produced for said internal butterfly circuit, followed by μ-p-3 zero bits at the end of the number; and[[,]]

[[-]]if p+1>μ-2, the number formed by the p+1 low-order bits of the second binary address produced for said internal butterfly circuit, minus the [[its]] μ-p-1 low-order bits of the second binary address.

29. (Currently Amended) The calculation method according to claim 44, wherein ~~in turn dependent on claim 3, in turn dependent on claim 2, characterized in that~~ in each transformation step E_P, the butterfly circuits ~~butterflies~~ are distributed among 2^P calculation blocks,

wherein [[that]] each calculation block comprises one peripheral butterfly circuit and $N/2^{p+2}$-1 internal butterfly circuits ~~butterflies~~, and

wherein [[that]] the peripheral butterfly circuit of the rank α calculation block in transformation step E_β transforms the input samples of rank $2^{\mu-\beta}\alpha$, $2^{\mu-\beta}\alpha+2^{\mu-\beta-1}-1$, $2^{\mu-\beta}\alpha+2^{\mu-\beta-1}$, $2^{\mu-\beta}\alpha+2^{\mu-\beta}-1$ into output samples of the same rank,

and wherein [[that]] the internal rank τ butterfly circuit of the rank α calculation block in transformation step E_β transforms the input samples of rank $2^{\mu-\beta}\alpha+2\tau+1$, $2^{\mu-\beta}\alpha+2\tau+2$, $2^{\mu-\beta}\alpha+22^{\mu-\beta-1}-2\tau-3$, $2^{\mu-\beta}\alpha+22^{\mu-\beta-1}-2\tau-2$ into output samples of the same rank.

30. (Currently Amended) The calculation method according to claim 29, ~~characterized in~~ further comprising a final step of modifying the sequence of the output samples provided in the last transformation step and classifying the output samples [[them]] in ascending order of index n.

31. (Currently Amended) The calculation method according to claim 29, wherein ~~characterized in that~~ each butterfly circuit is assigned a coefficient W^S, whereon the calculation inside the butterfly is based, said coefficient [[being]] equal to $e^{-j(2\pi s/N)}$ with $s \in [0..N/4-1]$ for a fast Fourier transform, and said coefficient [[is]] equal to $e^{j(2\pi s/N)}$ with $s \in [0..N/4-1]$ for an inverse fast Fourier transform.

32. (Currently Amended) The calculation ~~Calculation~~ method according to claim 31, wherein ~~characterized in that~~ the internal rank τ butterfly circuit of the rank α calculation block in transformation step E_β is assigned coefficient W^δ with $\delta = (\tau + 1).\ 2^\beta$.

33. (Currently Amended) The calculation method according to claim 32, wherein ~~characterized in that~~ the butterfly circuits ~~butterflies~~ for implementing the transformation steps are all of the same type and [[have]] comprise:

[[-]]four inputs for receiving input samples and four outputs for providing output samples, and

[[-]]four additional inputs, respectively primary mode, secondary mode, permutation, and coefficient inputs,

in order to selectively apply different transformation operations to the input samples, each operation being determined by the values assigned to the primary mode, secondary mode, permutation signals, and a coefficient admitted on said corresponding additional inputs.

34. (Currently Amended) The calculation method according to claim 33, wherein ~~characterized in that~~, for each butterfly circuit, the primary mode signal is 0 for a peripheral butterfly circuit and 1 for an internal butterfly circuit,

in that the permutation signal is 0 for the even rank calculation blocks, including rank 0, and 1 for the odd values.

35. (Currently Amended) The calculation method according to claim 31, wherein characterized in that the secondary mode signal is 1 if the butterfly circuit, whether [[be it]] peripheral or internal, is used for the first transformation step, and otherwise 0.

36. (Currently Amended) The calculation method according to claim 35, wherein ~~characterized in that~~, for four input samples e1, e2, e3, and e4, and for a complex coefficient W^S=A+j.B, the butterfly circuit delivers the following output samples s1, s2, s3, and s4:

1) if the primary mode and secondary mode signals are 0:

s1 = (e1 + e2) /2,

s2 = (e1 – e2) /2,

s3 = (e4 – e3) /2, and

s4 = (e3 + e4) /2;

2) if the primary mode signal is 0 and the secondary mode signal is 1:

s1 = [(e1 + e4) /2-e2] /2,

s2 = [e1 + e4) /2-e2] /2,

s3 = [e3 – (e1 – e4) /2] /2, and

s4 = [e3+ (e1 + e4) /2]/2;

3) if the primary mode signal is 1 and the permutation signal is 0:

s1 = (e1 +e3)/2,

s2 = (e2+e4)/2,

s3 = [(e1-e3).A – (e2+e4).B]/2, and

s4 = [-(e1-e3).B + (e2+e4).A]/2;

4) if the primary mode signal is 1 and the permutation signal is 1:

s1 = [(e1 =- e3).A – (e2 +e4).B]/2,

s2 = [-(e1-e3).B + (e2+e4).A]/2,

s3 = (1+e3)/2, and

s4 = (e2-e4)/2.

37. (Currently Amended) The calculation method according to claim 33, wherein ~~characterized in that~~ the first and second binary addresses of μ bits are generated for each butterfly circuit, each binary address corresponding to the rank of an input sample of said butterfly circuit and the second binary address being greater than the first binary address.

38. (Currently Amended) The calculation method according to claim 37, wherein ~~characterized in that~~ said first and second binary addresses are consecutive and an internal butterfly circuit is involved.

39. (Currently Amended) The calculation method according to claim 37, wherein ~~characterized in that~~, if a peripheral butterfly circuit is involved, the μ-p low-order bits of the first address are equal to 0, and the μ-p low-order bits of the of the second address form a number equal to $N/2^{p+1}-1$.

40. (Currently Amended) The calculation method according to claim 38, wherein ~~characterized in that~~ the address of the two other samples to be applied to the inputs of the butterfly circuit are obtained by inverting the μ-p low-order bits of both produced addresses.

41. (Currently Amended) The calculation method according to claim 40, wherein ~~characterized in that~~ even-numbered address samples and odd-numbered address samples are stored in two separate memories.

42. (Currently Amended) The calculation method according to claim 41, wherein ~~characterized in that~~ the value of the parameter s of the coefficient W^S assigned to an internal butterfly circuit in transformation step E_P is coded by μ-2 bits, and is:

[[-]]if $\mu-p-1=\mu-2$, the number formed by the μ-p-1 low-order bits of the second address produced for said internal butterfly circuit;[[,]]

[[-]]if $\mu-p-1<\mu-2$, the number formed by the μ-p-1 low-order bits of the second address produced for said internal butterfly circuit, followed by p-1 zero bits at the end of the number; and[[,]]

[[-]]if $\mu-p-1>\mu-2$, the number by the μ-p-1 low-order bits of the second address produced for said internal butterfly circuit, minus the [[its]] p+1 low-order bits of the second address.

Please add new claims 43 and 44 as follows:

43. (New) The calculation method according to claim 2, wherein, in each transformation step, each butterfly circuit transforms input sample pairs, the ranks of the input samples of the same pair within the series of input samples of said transformation step being symmetrical with respect to a center between the end rank values of the input samples transformed by said butterfly circuit.

44. (New) The calculation method according to claim 43, further comprising the step of:

transforming input samples into output samples in μ-1 transformation steps E_P, wherein

$\mu = \log_2(N)$ and $p \in [0..\mu-2]$.